Agilent ParBERT 81250

Agilent N4872A ParBERT 13.5 Gbps Generator
Agilent N4873A ParBERT 13.5 Gbps Analyzer

Technical Specifications

Version 1.0

General

The N4872A Generator and N4873A Analyzer modules are each one VXI slot wide and operate in a range from 620 Mbps up to 13.5 Gbps. The ParBERT 13.5 Gbps modules require the E4809A 13.5 GHz Central Clock module, which covers two VXI slots. All specifications, if not otherwise stated, are valid at the end of the recommended N4910A cable set (24" matched pair 2.4mm).

The N4872A Generator module generates hardware-based PRBS up to 2^{31}-1, PRWS and user-defined patterns and provides a memory depth of 64 Mbit. The N4873A can synchronize on a 48bit detect word, or on a pure PRBS pattern without detect word.

Timing Specifications

The ParBERT 13.5 Gbps modules are able to work with three different clock modes.
- *Internal Clock Mode:* The common clock mode is provided by the E4809A 13.5 GHz Central Clock module, which generates clock frequencies up to 13.5 GHz.
- *External Clock Mode:* The system also works synchronously with an external clock, which is connected to the E4809A clock module.

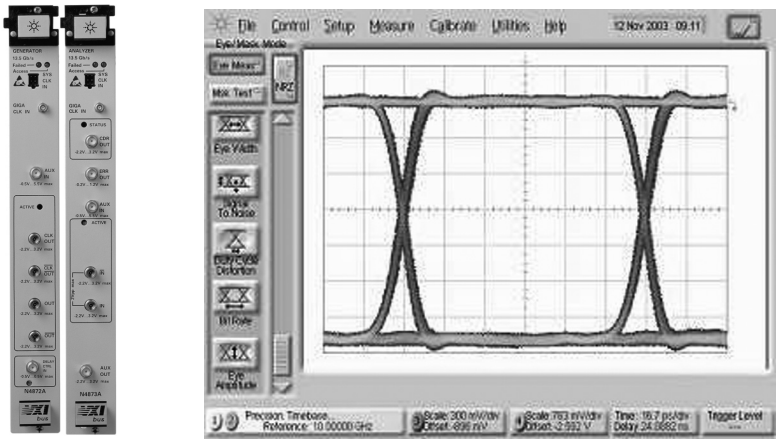

Figure 1: N4872A & N4873A and waveform

Table 1: N4872A Data Generator Timing Specifications (@ 50 % of amplitude, 50Ohm to GND)

Frequency range	620 MHz to 13.500 GHz
Delay = Start delay+Fine delay	Can be specified as leading edge delay in fraction of bits in each channel
Start Delay Range	0 to 100ns
Fine Delay Range	+/- 1Period (can be changed without stopping)
Delay Resolution	100 fs
Accuracy	±10 ps ± 20 ppm relative to the zero-delay placement. (@ 25°C - 40°C ambient temp.)
Relative Delay Accuracy	2ps + 2% typ. (@ 25°C - 40°C ambient temp.)
Skew between modules of same type	20 ps after deskewing at customer levels and unchanged system frequency. (@ 25°C - 40°C ambient temp.)

- *CDR Mode:* Using the N4873A 13.5 Gbps Analyzer CDR capabilities, it is required to connect the Analyzer's CDR Out to the E4809A Clock Module's Clock In.

Sequencing

The sequencer receives instructions from the central sequencer and generates a sequence according to that. The channel sequencer can generate a sequence with up to 120 segments. The sequencer has 2 loop levels, which allow nested loops.

An analyzer channel generates feedback signals that can control the channel sequencer and/or the central sequencer. In the case of parallel analyzer channels, the feedback has to be routed to the central sequencer to allow a common reaction of all parallel channels. In the case of a single receive channel, the channel sequencer itself can handle the feedback signals.

Pattern Generation

The data stream is composed of segments. A segment can be made up of the memory-based pattern type, memory-based PRBS or hardware generated PRBS. A total of 64Mbit (at segment length resolution 512bits) are available for memory-based pattern and PRBS.

Memory-based PRBS is limited to 2^{15}-1 or shorter. Memory-based PRBS allows special PRBS modes like zero substitution (also known as extended zero run) and variable mark ratio.

A zero substitution pattern extends the longest zero series by a user selectable number of additional zeroes. The next bit following these zero series will be forced to 1. Mark ratio is the ratio of 1s and 0s in a PRBS stream, which is 1/2 in a normal PRBS. Variable mark ratio allows values of 1/8, 1/4, 1/2, 3/4 and 7/8.

Due to granularity reasons a PRBS has to be written to RAM several times, at a multiplexing factor of 512 the number of repetitions is also 512. That means that a 2^{15}-1 PRBS uses up to 16Mbit of the memory. Hardware-based PRBS can be a polynomial up to a degree of 2^{31}-1. No memory is used so is available for memory-based pattern generation. Error insertion allows inserting single or multiple errors into a data stream. In case of an error a bit will be inverted, so instead of a 0 a 1 is generated and vice versa.

Table 2: N4872A Pattern and Sequencing

Patterns:	
Memory-based	
PRBS/PRWS	Up to 64Mbit
Marker Density	2^n-1, n= 7, 9, 10, 11, 15
Errored PRBS/PRWS	1/8, 1/4, 1/2, 3/4, 7/8 at 2^n-1, n= 7, 9, 10, 11, 15
Extended ones or zeros	2^n-1, n= 7, 9, 10, 11, 15
Hardware-based	
PRBS	2^n-1, n= 7, 10, 11, 15, 23, 31
PRWS Port width	1, 2 , 4, 8, 16

Table 3: Data rate range, segment length resolution, available memory for synchronisation and fine delay operation

Data rate rangeMbit/s	Segment length resolution	Maximum memory depth, bits
620 ... 1.350,000	32 bits	4.194,304
620 ... 2.700,000	64 bits	8.388,608
620 ... 5.400,000	128 bits	16.777.216
620 ... 10.800,000	256bits	33.554.432
620 ... 13.500,000	512 bits	67.108.864

N4872A Generator Module

The N4872A generates differential or single-ended data and clock signals operating from 620 Mbps up to 13.5 Gbps. The output levels are able to drive high-speed devices with interfaces like LVDS, ECL, PECL, CML and low voltage CMOS. The nominal output impedance is 50 Ohm typical. The Delay Control IN has a single-ended input with 50 Ohm impedance. The input voltage allows one to modulate a delay element up to 1 GHz (200ps) within the Generator's differential output.

The AUX IN has a single-ended input with a 50 Ohm impedance. The AUX IN allows injecting gating signals.
An active (TTL high) signal at the auxiliary input forces (gates) the data to a logic zero.

Data OUT

Table 3: Parameters for N4872A ParBERT 13.5 Gbps Generator

Data Output	1, differential or single ended, 2.4mm(f)	**(1)**
Range of Operation	620 Mbps - 13.5 Gbps	
Impedance	50 Ohm typ.	
Output amplitude/Resolution	0.1Vpp – 1.8 Vpp / 5mV	
Output voltage window	-2.00 to +3.00 V	
Short circuit current	72 mA max.	
External termination voltage	-2V to +3V	**(2)**
Data formats	Data: NRZ, DNRZ	
Addressable technologies	LVDS, CML PECL; ECL (terminated to 1.3V/0 V/-2 V) low voltage CMOS	
Transition times (10%-90%)	<25ps	
Jitter	9 ps peak-peak typ.	**(3)**
Cross-point adjustment	20%...80% typ.	
(Duty cycle distortion)		

(1) In single-ended mode, the unused output must be terminated with 50 Ohm to GND.
(2) External termination voltage must be less than 3V below V_{OH}. External termination voltage must be less than 3V above V_{OL}. Termination into AC is possible.
(3) Clock Out to Data Out

Clock OUT

Table 4: Parameters for N4872A ParBERT 13.5 Gbps Generator

Clock Output	1, differential or single-ended, 2.4mm(f)	**(1)**
Frequency	620 MHz - 13.5 GHz	
Impedance	50 Ohm typ.	
Output amplitude/Resolution	0.1Vpp – 1.8 Vpp / 5mV	
Output voltage window	-2.00 to +2.80 V	
Short circuit current	72 mA max.	
External termination voltage	-2V to +3V	**(2)**
Addressable technologies	LVDS, CML PECL; ECL (terminated to 1.3V/0 V/-2 V) low voltage CMOS	
Transition times (20%-80%)	<20ps pp	
Jitter	1 ps RMS typ.	
SSB phase noise (10GHz@ 10kHz offset, 1Hz bandwidth)	< - 75dBc with clock module E4809A typ.	

(1) In single-ended mode, the unused output must be terminated with 50 Ohm to GND.
(2) External termination voltage must be less than 3V below V_{OH}. External termination voltage must be less than 3V above V_{OL}. Termination into AC is possible.

Delay Control IN

Table 5: Parameters for N4872A ParBERT 13.5 Gbps Generator

Delay Control Input	Single-ended; DC-coupled; SMA(f)
Input voltage window	-250mV ... +250mV (DC-coupled)
Input Impedance	50 Ohm typ.
Data Rate	
Delay Range	-100ps ... +100ps
Modulation Bandwidth	DC ... 1 GHz @ < 10.5 Gbps

AUX IN

Table 6: Parameters for N4872A ParBERT 13.5 Gbps Generator

Interface	DC Coupled, 50 Ω nominal
Levels	TTL levels
Minimum Pulse Width	100 ns
Connector	SMA female

N4873A Analyzer Module

The analyzer features are:
- Acquire data from start
- Compare and acquire data around error
- Compare and count erroneous ones and zeros to calculate the Bit-Error-Rate.

Receive memory for acquired data is up to 64Mbit deep, depending on segment length resolution. The stimulus portion of the channel generates expected data and mask data. Mask data is also available at the maximum Mux-factor (16, 32, 64, 128, 256, 512).

The analyzer is able to synchronize on a received data stream by means of a user selectable synchronization word. The sync. word has a length of 48 bits and is composed of zeros, ones and Xs (don't cares). The detect word must be unique within the data stream. Synchronization on a pure PRBS data-stream is done without a detect-word, instead by simply loading a number of the incoming bits into the internal PRBS generator. A pre-condition for this is that the polynomial of the received PRBS is known.

The input comparator has differential inputs with 50 Ohm impedance. The sensitivity of 50mV and the common mode range of the comparator allow the testing of all common differential high-speed devices. The user has the choice of using the differential input with or without termination voltage or as single-ended input (with termination voltage). The differential mode does not need a threshold voltage, whereas the single-ended mode does. But also in differential mode the user can select one of the two inputs and compare the signal to a threshold voltage.

Table 7: N4873A Analyzer Timing All timing parameters are measured at ECL levels, terminated with 50Ohm to GND

Sampling rate	620 MHz to 13.500 GHz
Sample Delay	Can be specified as leading edge delay in frac tion of bits in each channel
Start Delay Range	0 to 100 ns
Fine Delay Range	+/- 1Period (can be changed without stopping)
Delay Resolution	Same as generator
Accuracy	±10 ps ± 50 ppm relative to the zero-delay placement. **(1)**
Relative Delay Accuracy	2 ps ± 2%
Skew between modules of same type	20 ps after deskewing at customer levels and unchanged system frequency. **(1)**

(1) Temperature

Table 8: N4873A Pattern and Sequencing

Analyzer Auto-synchronization	On PRBS or Memory-based Data Manual or automatic by: Bit synchronization with or without automatic phase alignment Automatic delay alignment around a start sample delay (Range: ± 50 ns) BER Threshold: 10^{-4} to 10^{-9}

Data IN

Table 9: Parameters for N4873A ParBERT 13.5 Gbps Analyzer

Number of channels	1, differential or single ended, 2.4mm (f)
Range of Operation	620 Mbps - 13.5 Gbps
Max Input amplitude	2Vpp
Input sensitivity	50 mVpp typical @ 10 Gbps, PRBS 2^{31} -1, and BER 10^{-12}
Input voltage range	-2V ... +3 (selectable 2V window)
Internal termination voltage (can be switched off)	-2.0 to +3.0 V (must be within selected 2V window)
Threshold voltage range	-2.0 to + 3.0 V (must be within selected 2V window)
Threshold resolution	0.1 mV
Minimum detectable pulse width	25ps typ.
Phase margin (Source: N4872A)	1UI - 12ps typ.
Impedance	50 Ohm typ. (100 Ohm differential, if termination voltage is switched off)

Clock Data Recovery

The Analyzer module has integrated CDR capabilities, which allow the recovery of either clock or data. Before the CDR can lock onto the incoming data stream, the data rate must be defined within the user interface; common data rates are pre-defined. In CDR mode, phase alignment to the center of the eye is done automatically during synchronization. To ensure correct operation, the CDR Output must be connected to the Clock Input of the E4809A 13.5 GHz Central Clock module.

Table 10: Parameters for N4873A ParBERT 13.5 Gbps Analyzer - Clock Data Recovery

Common Data Rates	OC-192:	9.953Gbps
	10GbE:	10.3125Gbps
	Fiber Channel:	10.51875 Gbps
	G.709/G.975:	10.664Gbps / 10.709Gbps
	S-ATA/FireWire:	6.4Gbps
	PCI-Express:	6.4Gbps
	OC-48:	2.488Gbps
	10GbE:	3.125Gbps
	SAN:	3.187Gbps
	S-ATA/FireWire:	3.2Gbps
Frequency Ranges	9.9 GHz ...10.90 GHz	
	4.23 GHz ... 6.40 GHz	
	2.115 GHz ... 3.20 GHz	

AUX OUT

The AUX OUT provides data or recovered clock signals.

Table 11: Parameters for N4873A 13.5 Gbps Analyzer - AUX OUT

Interface	AC Coupled, 50 Ω nominal
Amplitude	600 mV nominal
Output Jitter (Clock @ AUX OUT)	0.01 UI rms typical
Connector	SMA female

Ordering Information

N4872A	ParBERT 13.5 Gbps Generator Module
N4873A	ParBERT 13.5 Gbps Analyzer Module
E4809A	13.5 GHz Central Clock Module

Accessories:

N4910A	2.4mm match cable pair
N4912A	2.4mm 50Ohm termination male connector
N4913A	4 GHz deskew probe for E4809A

Technical Specifications

All specifications describe the instrument's warranted performance. Non-warranted values are described as typical. All specifications are valid from 10° to 40° ambient temperature after a 30 minute warm-up phase, with outputs and inputs terminated with 50 Ohms to ground at ECL levels if not specified otherwise.

Related Literature	Publication Number
• Agilent ParBERT 81250 Parallel Bit Error Ratio Tester, Product Overview	5968-9188E
· 10GbE Technology and Device Charaterization, Product Note	5988-6960EN
· Agilent ParBERT 81250 13.5 Gb/s Parallel Bit Error Ratio Test Platform, Photocard	5988-9201EN

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